REMARKS

Reconsideration of this application, as presently amended, is respectfully requested. Claims 1-16 are now pending in this application, new claims 10-16 having been added by the present Amendment. Claims 1 and 4 stand rejected. Claims 2, 3 and 5-9 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

New independent claims 10-16 correspond to claims 2, 3 and 5-9, respectively, rewritten in independent form. Accordingly, claims 10-16 should be in condition for allowance.

Claim Rejections – 35 U.S.C. §102

Claims 1 and 4 were rejected under 35 U.S.C. §102(a) as being anticipated by **Fujita et al.** (Japanese Patent Publication 2002-124877). For the reasons set forth in detail below, this rejection is respectfully traversed.

Claims 1 and 4 have been amended to further recite "wherein a predetermined value is subtracted from the input signal such that the output of the amplifier is controlled in a linear area without being saturated". Support for this change is provided, e.g., on page 7, lines 9-20 of the application specification.

The **Fujita et al.** reference is directed to an A/D conversion circuit for a solid state image sensor. As shown in Fig. 1, the A/D conversion circuit includes M units (U1-UM), each unit having two or more photodiodes PD. An integrator 10 receives a current signal from a photodiode, integrates the current signal and outputs an analog voltage value A1.

A first analog-to-digital converter (ADC) 20 converts the analog voltage value A1 to a first 8-bit digital value D_{11}-D_4 and outputs the 8-bit digital value. The ADC 20 also outputs a voltage value A2 corresponding to a difference between an analog value corresponding to the first 8-bit digital value D_{11}-D_4 and the analog voltage value A1. The voltage value A2 is output to an amplifier 30 that amplifies the value A2. The amplified value A2 is input to an ADC circuit 40 that converts the input to a 4-bit digital value D_3-D_0.

However, it is submitted that **Fujita et al.** does not disclose or suggest subtracting a predetermined value from the input signal of the amplifier such that the output of the amplifier is controlled in a linear area without being saturated. In particular, Fig. 1 of **Fujita et al.** shows ADC 20, amplifier 30 and ADC 40. ADC 20 receives a signal from PDs through integrating circuit 10. ADC 40 is connected to ADC 20 through SW2 and amplifier 30. Amplifier 30 processes a signal from ADC 20 to generate an amplified version of the received signal, and controller 50 controls this amplification in amplifier 30. Since controller 50 does not receive any signal from ADC 20, amplifier 30 or ADC 40, a predetermined value cannot be subtracted from the input signal to avoid saturation in the output of the amplifier 30 and the output of the the amplifier 30 cannot be controlled in a linear area.

In view of the above amendments and remarks, it is submitted that claims 1 and 4 patentably distinguish over the **Fujita et al.** reference. Reconsideration and withdrawal of the rejection under §102 are respectfully requested.

CONCLUSION

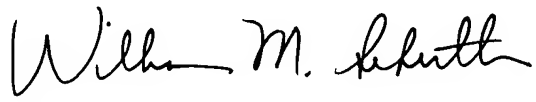
In view of the foregoing amendments and accompanying remarks, it is submitted that all pending claims are in condition for allowance. A prompt and favorable reconsideration of the rejection and an indication of allowability of all pending claims are earnestly solicited.

If the Examiner believes that there are issues remaining to be resolved in this application, the Examiner is invited to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite and complete prosecution of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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